UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/489,652	01/24/2000	William G. Burroughs	KUC-718US	6089

46900 7590 06/06/2005

MENDELSOHN & ASSOCIATES, P.C.
1500 JOHN F. KENNEDY BLVD., SUITE 405
PHILADELPHIA, PA 19102

EXAMINER	
TANG, KENNETH	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/489,652	BURROUGHS ET AL.	
	Examiner	Art Unit	
	Kenneth Tang	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

KC

PD

DETAILED ACTION

1. This action is in response to the Amendment filed on 3/4/05. Applicant's arguments have been fully considered but were not found to be persuasive.

2. Claims 27-52 are presented for Examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 27-30 and 33-51 rejected under 35 U.S.C. 102(b) as being anticipated by Milton et al. (hereinafter Milton) (US 4,862,452).

4. As to claim 27, Milton teaches in a system comprising a first processor (DSP module) and one or more other processors (plurality of DSP modules), a method for applying one or more interrupt signals to the one or more other processors (interrupt handshaking scheme) *(see Abstract, col. 1, lines 58-68, col. 2, lines 21-63)*, the method comprising:

(a) generating, in the first processor, a data signal having one or more data bits is inherent because the DSP sends a signal of data *(col. 2, lines 21-63)*;

(b) transmitting the data signal from a data port of the first processor to a signal unit external to the first processor and the one or more other processors *(col. 2, lines 43-53)*;

(c) converting, in the signal unit, the data signal into one or more interrupt signals, wherein each data bit in the data signal corresponds to a different interrupt signal (Digital to Analog or Analog to Digital or serial to parallel, etc.) *(col. 2, lines 21-35 and 43-53)*; and

(d) transmitting each interrupt signal from the signal unit to an interrupt port of an other processor (interrupt handshaking scheme, switch and main controller) *(col. 2, lines 21-63, col. 1, lines 58-68)*.

5. As to claim 28, Milton teaches wherein the data signal has a plurality of data bits is inherent because of the same reasons as shown in claim 27; the signal unit converts the data signal into a plurality of interrupt signals *(col. 2, lines 21-35 and 43-53)*; and each interrupt signal is transmitted to a different interrupt port of an other processor (interrupt handshaking scheme, switch and main controller) *(col. 2, lines 21-63, col. 1, lines 58-68)*.

6. As to claim 29, Milton teaches wherein at least two interrupt signals are transmitted to two different ports of a single other processor *(col. 2, lines 21-63, col. 1, lines 58-68)*.

7. As to claim 30, Milton teaches wherein at least two interrupt signals are transmitted to interrupt ports of at least two different other processors (bidirectional communication between plurality of DSP modules) *(col. 2, lines 21-63, col. 1, lines 58-68)*.

10. As to claim 33, Milton teaches the first processor transmits an address signal to the signal unit; and the signal unit compares the address signal to a specified value to determine whether to

store the two sequential values in the two registers *(col. 1, lines 58-68, col. 4, lines 44-55)*.

11. As to claim 34, Milton teaches wherein each interrupt signal is transmitted from the signal unit to a corresponding interrupt port of a corresponding other processor via a dedicated line *(col. 1, lines 27-42)*.

12. As to claim 35, Milton teaches wherein the data signal is transmitted from the first processor to the signal unit via a shared data bus (bidirectional PCM links) *(col. 2, lines 21-63, col. 1, lines 58-68)*.

13. As to claim 36, it is rejected for the same reasons as stated in the rejection of claim 27. As aleady shown, Milton teaches switching and bidirectional communication of DSP modules *(col. 2, lines 21-63, col. 1, lines 58-68)*.

14. As to claim 37, Milton teaches wherein at least one other interrupt signal is transmitted from the other signal unit to an interrupt port of at least one other processor *(col. 2, lines 21-63, col. 1, lines 58-68)*.

15. As to claims 38-48, they are rejected for the same reasons as stated in the rejections of claims 27-37.

16. As to claims 49-50, they are rejected for the same reasons as stated in the rejections of

claims 1 and 35.

17. As to claim 51, it is rejected for the same reasons as stated in the rejection of claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 31-32 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Milton et al. (hereinafter Milton) (US 4,862,452) in view of Brown (US 3,896,418).

. As to claim 31, Milton fails to explicitly teach wherein the signal unit **detects** a transition in each data bit of the data signal over time to determine when to generate a corresponding interrupt signal. However, Brown teaches a system for providing an interrupt signal comprising a data bus coupled to the first processor for routing parallel bits of data *(Fig. 3a)*, a register and an edqe detector both coupled between the first and second processors *(col. 62, lines 7-10 and 42-43, col. 30, lines 13-29)*, the register coupled to the data bus for storing the parallel bits of data, at least one of the parallel bits of data having an active logic level *(col. 6, lines 38-63, col. 7, lines 45-56 and Abstract)*, where the edge detector coupled to the register for detecting active logic levels stored in the register and converting each active logic level into an interrupt signal *(col. 62, lines 7-19, col. 30, lines 13-29)*. Most importantly, the edge detector senses and detects

a transition in each data bit of the data signal over time to determine when to generate a corresponding interrupt signal *(col. 1, lines 26-48)*. It would have been obvious to combine Brown with Milton because it would provide the benefit of effective interrupt CPU operation and flexibility in design for various CPU systems *(col. 2, lines 34-48)*.

9. As to claim 32, it is rejected for the same reasons as stated in the rejection of claim 31. In addition, the edge detector detects a transition by: storing sequential values for the corresponding data bit in two registers; and comparing outputs from the two registers to detect a difference between the two sequential values *(col. 62, lines 7-19, col. 30, lines 13-29 and Abstract)*.

18. As to claim 52, it is rejected for the same reasons as stated in the rejections of claims 27, 34-35 and 38. In addition, Milton fails to explicitly teach detecting a transition in each data bit of the data signal over time to determine when to generate a coresponding interrupt signal. However, Brown teaches a system for providing an interrupt signal comprising a data bus coupled to the first processor for routing parallel bits of data *(Fig. 3a)*, a register and an edqe detector both coupled between the first and second processors *(col. 62, lines 7-10 and 42-43, col. 30, lines 13-29)*, the register coupled to the data bus for storing the parallel bits of data, at least one of the parallel bits of data having an active logic level *(col. 6, lines 38-63, col. 7, lines 45-56 and Abstract)*, where the edge detector coupled to the register for detecting active logic levels stored in the register and converting each active logic level into an interrupt signal *(col. 62, lines 7-19, col. 30, lines 13-29)*. Most importantly, the edge detector senses and detects a transition in each data bit of the data signal over time to determine when to generate a corresponding interrupt

signal *(col. 1, lines 26-48)*. It would have been obvious to combine Brown with Milton because it would provide the benefit of effective interrupt CPU operation and flexibility in design for various CPU systems *(col. 2, lines 34-48)*.

Response to Arguments

4. During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

5. Applicant argues on page 6 of the Remarks that neither Brown nor Milton does not teach or suggest a signal unit that converts a data signal transmitted from the data port of one processor into one or more interrupt signals that are applied to one or more interrupt ports of one or more other processors.

In response, the Examiner respectfully disagrees. It was shown in the rejection that Milton teaches a DSP signal processing system consisting of a plurality of DSP modules that converts data (from A/D, or D/A, or serial to parallel, etc.) and transmits data and interrupts to the ports of various DSP modules in a bidirectional manner *(see rejection of claim 27, for example)*.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kt
5/30/05

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100